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In the Claims:

Please amend claims 1, 5, 7, 10, 12 and 15 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A buffer management system for providing a plurality of independent buffers for use by an application, the system comprising:

a buffer memory, and

a controller[[,]] operably coupled to the buffer memory, ~~that is~~ the controller configured to partition the buffer memory into [[a]] the plurality of independent buffers[[,]] dependent upon a partition parameter received from the application that indicates ~~determines~~ a quantity of the plurality, wherein each buffer of the plurality of independent buffers has a buffer-size that is an integer power of two, to facilitate circular-access to the buffer.

2. (Previously Presented) The buffer management system of claim 1, wherein the controller is configured to include a circular-increment function that requires only an address-increment function and a bit-overwrite function to effect a circular-increment of a pointer to a select buffer of the plurality of independent buffers.

3. (Previously Presented) The buffer management system of claim 1, wherein the buffer-sizes of the plurality of independent buffers are equal.

4. (Previously Presented) The buffer management system of claim 1, wherein the controller is further configured to allocate the plurality of independent buffers among a plurality of source-destination paths.

5. (Currently Amended) The buffer management system of claim 1, wherein the controller is further configured to provide a write-interface and a read-interface to ~~one or more~~ the application[[s]], the write-interface ~~requiring only~~ receiving, from the application, an identification of data to be stored and an identification of a select buffer of the plurality of independent buffers to store the data and translating the identification of

the select buffer to an address corresponding to the select buffer, and the read-interface ~~requiring only~~ receiving, from the application, the identification of the select buffer, and translating the identification of the select buffer to an address corresponding to the select buffer.

6. (Previously Presented) The buffer management system of claim 1, wherein the buffer memory is addressed by an M-bit address, each buffer of the plurality of independent buffers is indexed by an N-bit index that forms a set of N most-significant-bits of the M-bit address, and the size of each buffer is at least 2^{M-N}.

7. (Currently Amended) A method of providing a plurality of independent buffers for use by an application ~~managing a buffer memory~~, the method comprising:

receiving, at a controller, a partition parameter from the application,

partitioning ~~the~~ a memory buffer into [[a]] the plurality of independent buffers, ~~wherein the plurality is determined from~~ based on the partition parameter, ~~and~~ wherein a size of each buffer of the plurality of independent buffers is an integer power of two, thereby facilitating circular-addressing of each buffer.

8. (Previously Presented) The method of claim 7, wherein the sizes of the plurality of independent buffers are equal.

9. (Previously Presented) The method of claim 7, further including providing circular-addressing for each buffer, wherein the circular-addressing includes: incrementing an address to the buffer memory, and overwriting select bits of the address, corresponding to an index to the buffer within the buffer memory.

10. (Currently Amended) The method of claim 7, further including:

providing a write-interface that ~~requiring only~~ receives, from the application, an identification of data to be stored and an identification of a select buffer of the plurality of independent buffers to store the data,

translating the identification of the select buffer into an address corresponding to the select buffer at which the data is to be stored, and

providing a read-interface that ~~requiring only~~ receives, from the application, the identification of the select buffer.

11. (Previously Presented) The method of claim 7, wherein the buffer memory is addressed by an M-bit address, each buffer of the plurality of independent buffers is indexed by an N-bit index that forms a set of N most-significant-bits of the M-bit address, and the size of each buffer is at least 2^{M-N}.

12. (Currently Amended) An integrated circuit for providing a plurality of buffers for use by an application, the circuit comprising

a buffer memory, and

a controller that includes write control logic[[,]] and read control logic, wherein the controller is configured to partition the buffer memory into [[a]] the plurality of buffers[[,]] based on a partition parameter that is provided to the controller by the application, each buffer of the plurality of buffers having a size that is an integer power of two, and the write control logic and read control logic are each configured to facilitate use of each buffer as a circular buffer.

13. (Previously Presented) The integrated circuit of claim 12, wherein the sizes of the plurality of buffers are equal.

14. (Previously Presented) The integrated circuit of claim 12, wherein the use of each buffer as a circular buffer requires circular-addressing, and the controller is configured to effect the circular-addressing via an incrementer that is configured to increment an address to the buffer memory, and a bit masker that is configured to overwrite select bits of the address, corresponding to an index to the buffer within the buffer memory.

15. (Currently Amended) The integrated circuit of claim 12, wherein the write control logic effects a storage of a data value to a select buffer of the plurality of buffers based

~~only~~ on an identification of the data value and an identification of the select buffer by translating the identification of the select buffer into an address corresponding to the select buffer at which the data is to be stored, and the read control logic effects a retrieval of the data value based ~~only~~ on the identification of the select buffer.

16. (Previously Presented) The integrated circuit of claim 12, wherein the buffer memory is addressed by an M-bit address, each buffer of the plurality of independent buffers is indexed by an N-bit index that forms a set of N most-significant-bits of the M-bit address, and the size of each buffer is at least 2^{M-N}.